Study of a grid-connected photovoltaic power conversion system with single-phase multilevel inverter

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in partial fulfillment of
ETLS 746 Power Electronics
University of St. Thomas
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Spring 2015
Due May 21, 2015

Abstract

This study seeks to verify the design of a grid-connected photovoltaic power conversion system with single-phase multilevel inverter (Beser et al., 2010). The modular design is expandable to allow for many voltage levels in the modified sine wave output. It also requires fewer switches than other common designs to create the same number of voltage levels. PSIM is used to model the inverter topology, first with DC voltage sources in place of PV arrays. Once the power requirements are determined for each PV module, a suitable number of PV arrays are selected and combined in series and in parallel. The resulting inverter with PV arrays is then simulated while transferring power to the grid (110 V-rms, 50 Hz). While power was converted effectively in this simulation and initially verified the results of Beser et al., closed loop control of the inverter was not achieved. This leaves some claims of the authors unverified.

Introduction

Interest in renewable energy continues to grow as people look for alternatives to the predominantly fossil fuel energy sources. In Minnesota, wind has been the most common source for renewable electrical power, with 8.9% of the state's total power generation coming from wind in 2010 (U.S. EIA, 2012). While solar energy has not yet played a large role in this state's energy economy, it has shown recent strong growth nationally. Solar power grew by 6.2 gigawatts in 2014, a 30 percent increase over the previous year and representing nearly $18 billion in new investment (Cusick, 2015). For integration into the existing AC power grid, DC photovoltaic (PV) arrays require inverters to convert the DC power into AC as efficiently as possible. The academic paper explored in this study, (Beser et al., 2010) presents a single-phase multi-level inverter topology for use in such a grid-connected application. The authors present it as having the benefit of requiring fewer switches to generate the same number of voltage levels of other common topologies. Personally, I was interested in this topic due to the possibility of implementing a microcontroller-based control scheme for the inverter. While I was unable to fully accomplish the control scheme described in the paper, I nevertheless learned a lot about joining DC energy sources to the AC power grid.

Details and discussion of results

Inverter topology

The authors of this paper present a topology for converting PV array DC voltage to AC for use in power grids. It is an expandable multilevel design, which allows for low harmonic content (THD) to be transferred to the grid. It can also be used in a standalone mode for providing power to a specific AC loads.

The topology contains three module types: the PV modules consisting of photovoltaic arrays and supporting capacitor banks, the level modules with switches to modify the DC-bus voltage, and the H-bridge module which acts to reverse the output voltage polarity every half-period. These modules are shown in Figure 1:

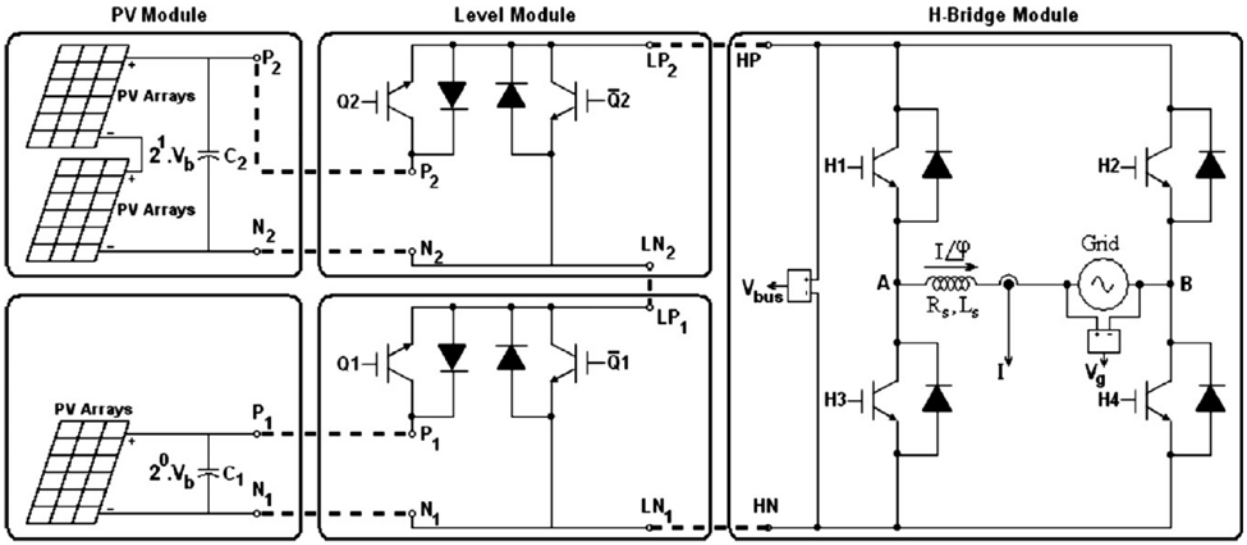

Fig. 1. Inverter module configuration with two level modules. (Beser et al., 2010)

The inverter is configured with *m* level modules. For the *k*th corresponding PV module, there are *k* PV arrays connected in series, each with base voltage V_b. This means that the 1st PV module has voltage V_b, the 2nd has voltage $2V_b$, the 3rd has $4V_b$, the 4th has $8V_b$, etc. Or, for the *k*th module ($k = 1, 2, 3, \ldots, m$):

$$V_{Ck} = 2^{(k-1)}V_b \quad (1).$$

Table 1

Q_1	Q_2	Q_3	Q_4		V_{bus}/V_b
0	0	0	0		0
1	0	0	0		1
0	1	0	0		2
1	1	0	0		3
0	0	1	0		4
1	0	1	0		5
0	1	1	0		6
1	1	1	0		7
0	0	0	1		8
1	0	0	1		9
0	1	0	1		10
1	1	0	1		11
0	0	1	1		12
1	0	1	1		13
0	1	1	1		14
1	1	1	1		15

The authors simulate and experimentally test an inverter with four level modules. This requires four switching signals, Q_1 – Q_4 (inverted to create $\overline{Q_1} - \overline{Q_4}$). Each level module can either provide V_{Ck} to the DC-bus voltage, or zero volts. This creates 15 different possible voltage levels stepping up by V_b. Together with zero and their negatives (voltages flipped by the H-bridge module), there are 31 voltage levels in the output waveform. Switching combinations are shown in Table 1.

Switching strategy

The switching strategy presented by Beser et al. presented me with some problems. First of all, they are based off a sinusoidal reference voltage

$$V_{ref} = V_{max} \sin(\omega t + \delta_{ref}) \quad (2).$$

Then, the given switching equations are

$$Q_1(t) = V_{ref}(t) \bmod 2 \quad (3)$$

$$Q_2(t) = \left(\frac{V_{ref}(t) - V_{ref}(t) \bmod 2}{2}\right) \bmod 2 \quad (4)$$

$$Q_k(t) = \left(\frac{V_{ref}(t) - V_{ref}(t) \bmod 2^{(k-1)}}{2^{(k-1)}}\right) \bmod 2 \quad (5).$$

My initial question was, "What do they mean by the modulus function?" The usual definition of *m* mod *n* is the remainder left over when *m* is divided by *n*. However, when you apply this definition to a continuous (analog) reference voltage of arbitrary magnitude, you get all sorts of decimal remainders with no resemblance to the binary switching signals presented by the authors (Figure 2).

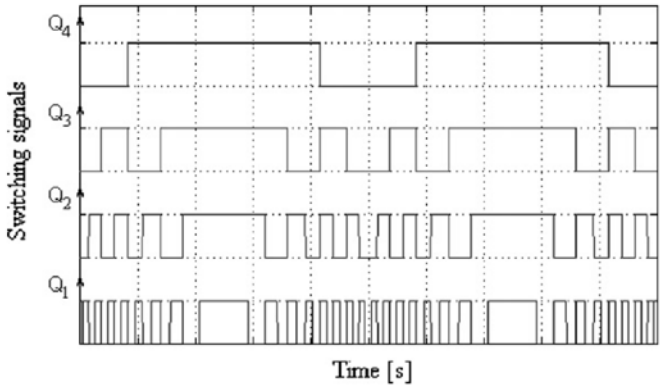

Fig. 2. Switching signals for the four level modules (Beser et al., 2010)

After looking at the given switching signals, it was clear that it was a kind of binary counter, with the width of each step selected to follow the reference sinusoid. This kind of counting would be possible if V_{ref} were instead made into an integer valued sine wave. Then V_{ref} mod 2 would take on the values of 0 or 1 only. If V_{max} = 15 V, then the reference voltage could be used in the switching equations to generate the desired switching signals.

So, to generate the switching signals I chose V_{max} = 15 V, rounded V_{ref} to the nearest integer, and took the absolute value (so that Q_k was always positive or zero). In a way, this created a kind of analog-to-digital-converter for the reference sinusoid. My simulated switching signals are shown in Figure 3. Note that they agree with the authors' figure.

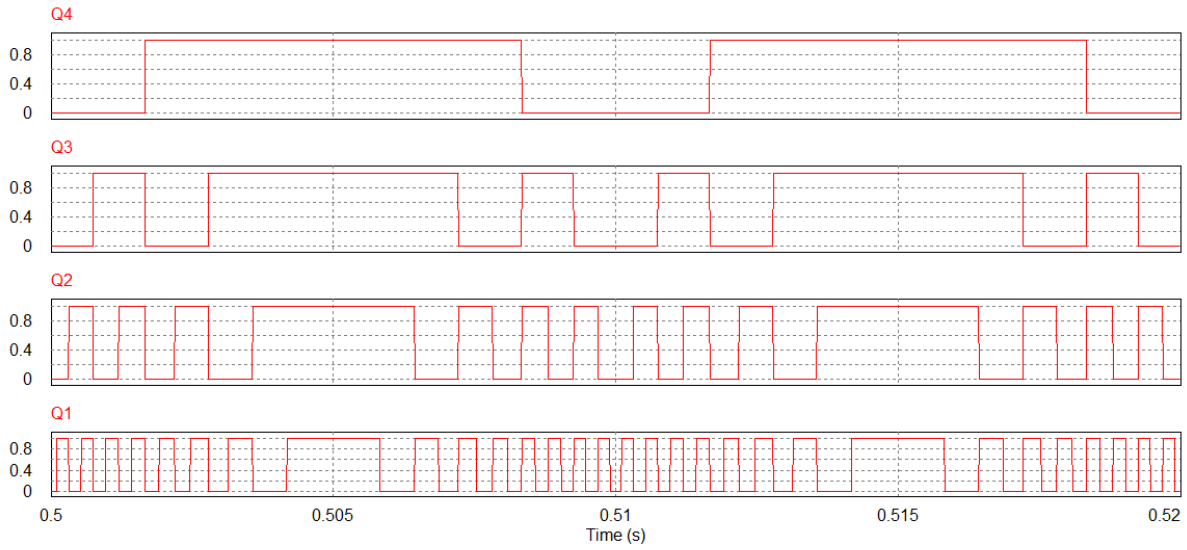

Fig. 3. Simulated switching signals from Simview, in agreement with the authors'

For the H-bridge module, V_{ref} was simply compared with ground to produce a square wave with frequency ω. This square wave was used to switch $H_1 - H_4$ and provide a fully AC output voltage. When $V_{ref} > 0$ the switches H_1 and H_4 are on (H_2 and H_3 off), and when $V_{ref} < 0$ the switches H_2 and H_3 are on (H_1 and H_4 off). The authors make no mention of PWM control of the H-bridge module, presumably since the level modules produce a nice modified sine wave with many small steps. Also, there is no filter on the output signal.

Topology simulation

The inverter topology was simulated using PSIM. To begin with, DC voltage sources were used in place of simulated solar arrays. V_b = 17.1 V was chosen in order to scale the level module voltages (17.1 V is the maximum power voltage given by the authors for the solar arrays used). The simulated inverter was constructed with ideal components as shown in Figure 4. Also included are voltage and sensor probes for monitoring load power and PV module power.

The authors simulated and experimentally built for a grid AC voltage of 110-V_{rms} at 50 Hz. The simulated waveform for V_o (V_{AB} in Figure 1) is given in Figure 5. Note that this waveform is in agreement with Beser et al.

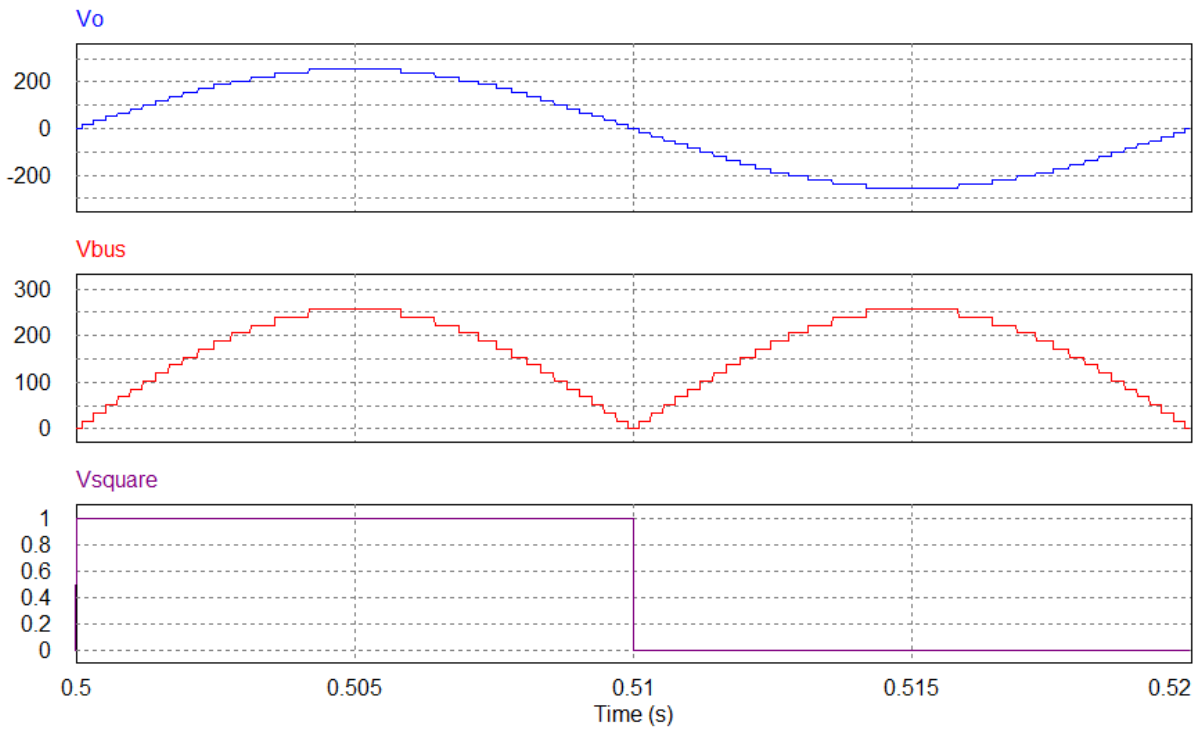

Fig. 5. Simulated output multilevel waveform V_o with 31 voltage levels. The output waveform V_o is in agreement with the authors' simulation

Next, to simulate the proposed system with PV arrays, the power produced by each PV module is determined in order to decide how many base arrays must be connected in series and in parallel so that no individual array is overpowered (asked to provide more power than it is capable of). Beser et al. designed for a 1 kW total output power. They selected base PV arrays with the following characteristics (Figure 6 and Table 2):

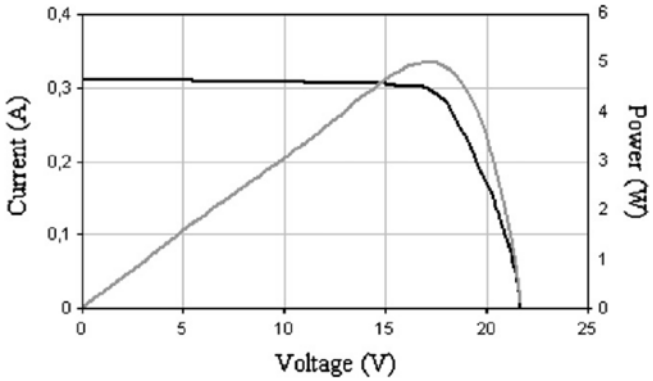

Fig. 6. I-V and P-V characteristics of the selected PV base array. (Beser et al., 2010)

Specifications of PV arrays.

Rated power (P_M)	5 W
Maximum power voltage (V_{PM})	17.1 V
Maximum power current (I_{PM})	0.30 A
Open-circuit power (V_{OC})	21.7 V
Short-circuit current (I_{SC})	0.31 A

Table 2. (Beser et al., 2010)

With the DC voltage source still standing in for simulated PV arrays, the inverter was run with various loads (resistive, inductive and capacitive). The real and reactive power delivered to the load was calculated, as well as the power produced by each DC source (Figure 7). My simulated results are summarized in Table 3.

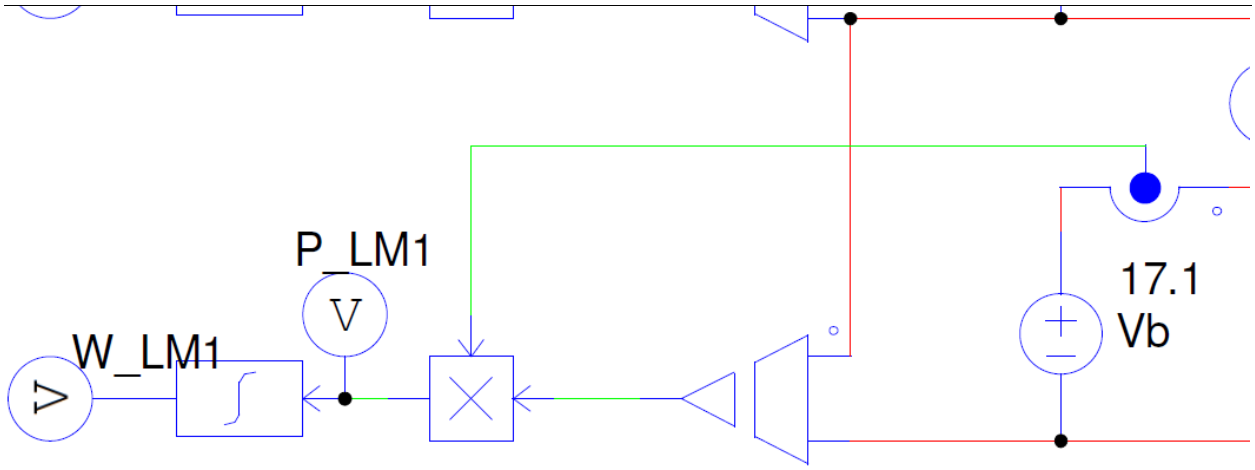

Fig. 7. Calculation of the level module energy and power in PSIM

Table 3. Level module and load energies for various loads													
PV array side								Load side			Series load		
W_{LM1} (J)	W_{LM2} (J)	W_{LM3} (J)	W_{LM4} (J)	W_{LMT} (J)	W_{LM2}/W_{LM1}	W_{LM3}/W_{LM1}	W_{LM4}/W_{LM1}	W_L (J)	P_L (W)	Q_L (VAr)	R (W)	X_L (W)	R_C (W)
0.491	1.116	2.547	5.899	10.052	2.274	5.191	12.023	10.052	497	0	65.76	-	-
0.981	2.232	5.093	11.798	20.104	2.274	5.191	12.023	20.103	1026	0	32.88	-	-
1.963	4.463	10.187	23.595	40.207	2.274	5.191	12.023	40.207	2034	0	16.44	-	-
0.302	0.687	1.569	3.637	6.195	2.277	5.200	12.053	6.181	309	463	32.88	49.32	-
0.853	1.940	4.427	10.253	17.473	2.274	5.189	12.018	17.463	869	-337	32.88	-	12.73

Table 3 is in very good agreement with the table in Beser et al. on page 2062 of the paper. Using the load closest to P_L = 1 kW, the power provided by each level module was calculated:

P_{LM1}	-49.06 W
P_{LM2}	-111.56 W
P_{LM3}	-254.63 W
P_{LM4}	-589.78 W

Table 4. Power provided by each level module for 1 kW load power

Note the calculated negative signs which indicate that each DC source was providing power (the calculated load powers in Table 3 were positive, indicating that the load consumed power). The results are also in good agreement with the power values given by the authors on page 2063.

It was already mentioned that to create different DC voltages for each level, each *k*th PV module would include $2^{(k-1)}$ base PV arrays in series. Each base array is rated for 5 W maximum output. If the required powers for each level from Table 4 are rounded to 50 W, 120 W, 260 W and 600 W, then the required numbers of base arrays for each PV level are:

(1 series x 10 parallel) x 5 W = 50 W for PV module 1 (6)
(2 series x 12 parallel) x 5 W = 120 W for PV module 2 (7)
(4 series x 13 parallel) x 5 W = 260 W for PV module 3 (8)
(8 series x 15 parallel) x 5 W = 600 W for PV module 4 (9).

In PSIM, I replaced the DC voltage sources with "Solar module (functional module)" arrays. This allowed me to enter all of the values from Table 2 so that the simulated solar array would produce the required I-V curves. In order to scale each array, I multiplied the voltages from Table 2 by the number of series arrays from Equations 6-9, and the currents by the number of parallel arrays from Equations 6-9. In this way each simulated array should be able to provide the required power to the inverter.

Finally, the reference sinusoidal voltage was shifted from a separate reference to the grid itself. That way, the inverter output V_o can be easily synchronized with V_{grid}. The completed simulated inverter is show in Figure 8.

Control scheme – WHERE'S THE KNOB?!

At this point, I sought to implement the control algorithm suggested by the paper's authors on pages 2060-61. However, there is a claim made by Beser et al. that I am unable to verify. They say that "the amplitude of the output voltage is easily regulated without modifying the number of level modules." They then show a graph with various waveforms (Beser et al., 2010, Fig. 9). The control scheme they outline seems to suggest that by a suitable choice of V_{ref} and δ_{ref}, you can modify V_o. I see how by changing ω of V_{ref}, the frequency of the output can be changed. I also understand how δ_{ref} can shift the phase of V_o. But I don't see how amplitude control is achieved. Sampling V_{ref} is simply used to calculate switching signals (or switching angles) for turning each level module on or off. The voltages of the PV modules are what determine how many volts are switched to the H-bridge module. So I'm left with the question, "WHERE'S THE KNOB FOR CONTROLLING AMPLITUDE?"

Searching out some other topologies, I found out that many designs use a buck or boost stage on the DC bus voltage coming from the solar panels to control the maximum power point (MPP) which occurs at the elbow of the P-V curve in Figure 6. Furthermore, Beser et al. don't discuss any kind of PWM control or filtering of the output. So again, no amplitude control!

Here is a block diagram of a different inverter design for reference:

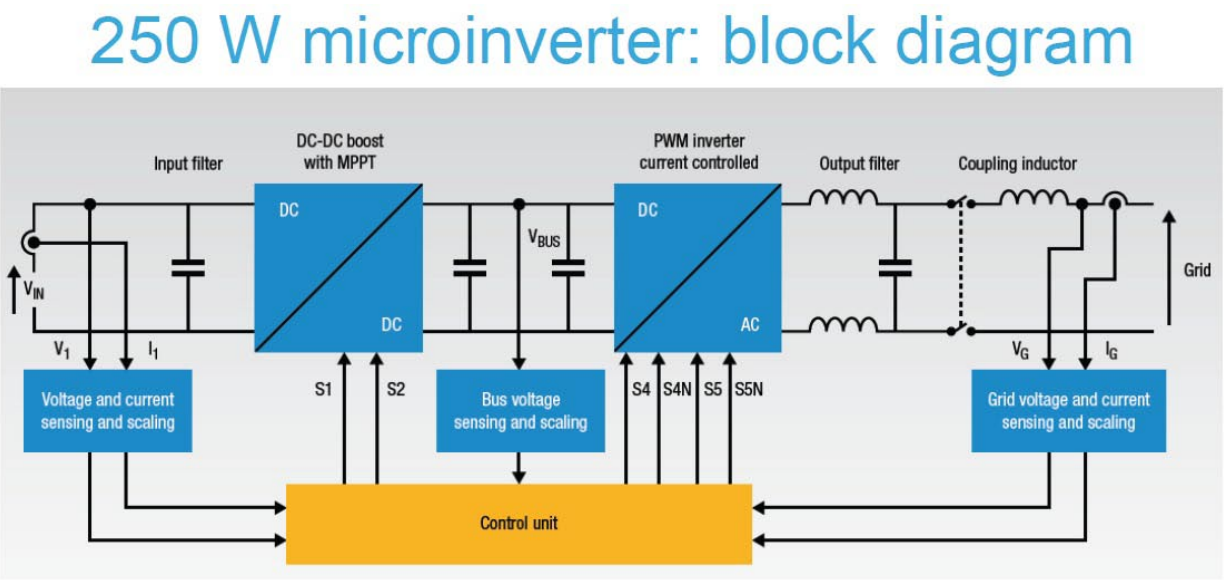

Fig. 8. The STEVAL-ISV003V1 microinverter available from Digikey. It utilizes both MPPT with a DC-DC boost stage, as well as PWM control. Both of these typical features are missing from Beser et al., 2010.

A problem with the authors' design is that there is no single bus voltage coming from the solar arrays, but rather a different DC voltage coming from each PV module. This leaves me wondering where I'd even try to implement a MPPT in the topology. Beser et al. give few details, saying that a "control algorithm is easily provided by a PIC18F452 microcontroller" and that "the MPPT procedure does not require any extra equipment, it consists of an algorithm." So, I was unable to implement the control scheme as presented in the paper.

I thought that perhaps by varying δ_{ref} I could achieve some kind of control over the output power as V_o shifted out of phase from V_{grid}. So I added a time delay block to delay the reference voltage that was created from the grid voltage. I did see some variation in the power delivered to the grid. Example graphs from Simview are given in Figure 9, and a summary of the simulations in Table 5.

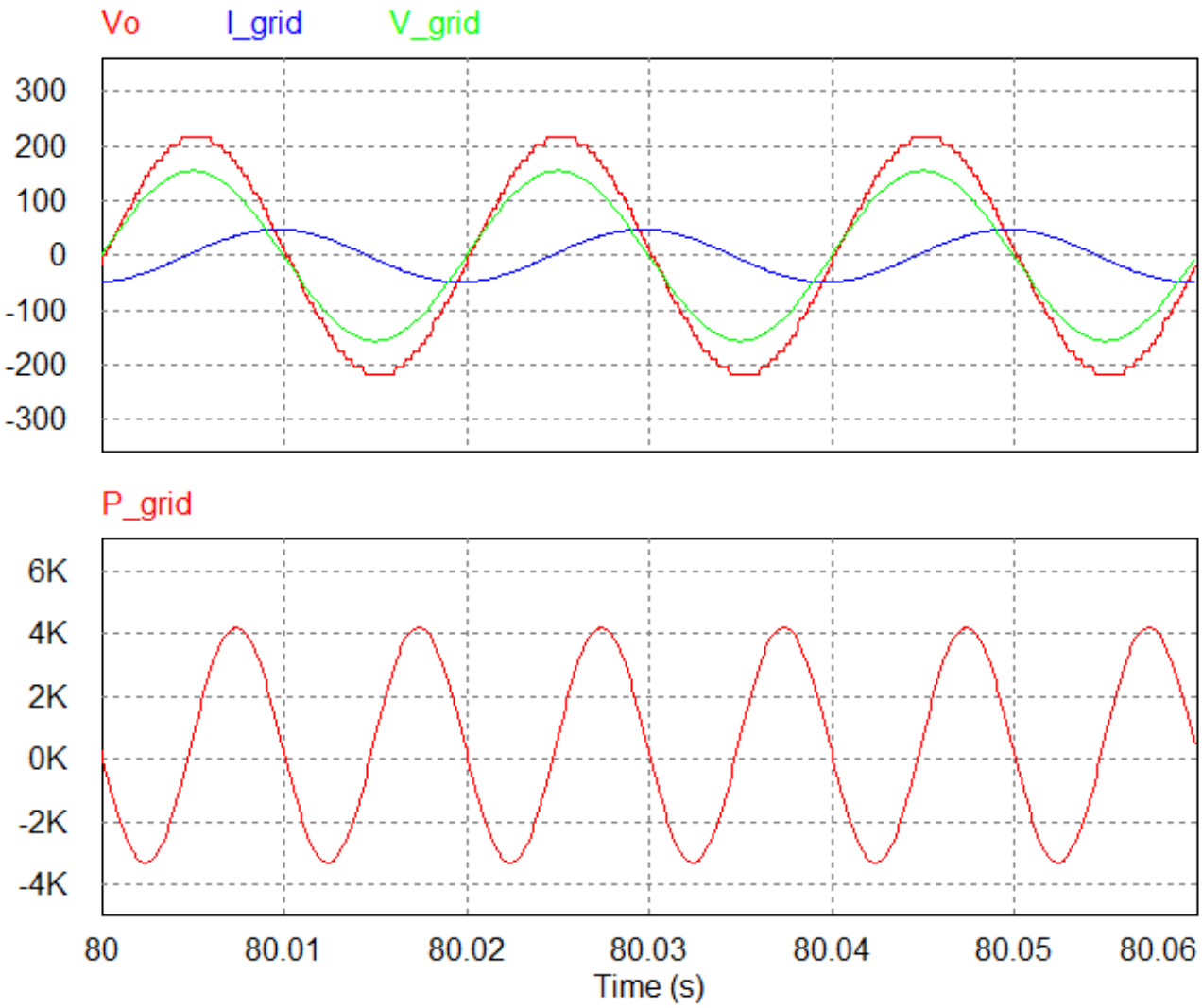

Fig. 9. Simulated output for the grid-connected inverter ($\delta_{ref} = 0$)

Table 5. Summary of simulation results with the grid-connect inverter

δ_{ref} (deg)	time delay (s)	P_{grid} (W)	V_o (V-rms)	I_{grid} (A-rms)	Q (VAr)
0.0	0	469.14	154.97	34.63	1507.21
-1.0	0.0000556	580.18	146.55	27.94	980.70
-1.8	0.0001000	470.22	154.96	34.62	1506.08
-3.6	0.0002000	267.89	165.42	43.05	2328.88
-10.8	0.0006000	-1180.87	198.01	70.93	6322.97

In the end, I was not able to attempt any kind of closed-loop control of this inverter design. Although I considered using δ_{ref} to try and control and maximize the power transferred to the grid, the method I used for creating this phase shift was unsuitable. By using a time delay, I could only adjust for negative phase shifts ($\delta_{ref} < 0$), not positive. Also, there did not seem to be a convenient method to have a variably controlled phase shift in PSIM. I considered writing a custom C-block, but determined that the amount of code required would be considerable. I left it

untried at this time. As such, I was not able to verify the various operating points that were tested by Beser et al.

Implications

The implications of this paper for further research remain to me unclear. The authors do not list any great benefits to their design beyond the fact that it may require fewer switches than other multilevel designs. If in fact the MPPT algorithm can be implemented without any other buck or boost stages, this would allow for a much simpler design while still providing high quality power in grid-connected applications.

Personally, I'd like to pursue the design of an inverter more along the lines of the one laid out in Figure 8. It more clearly contains "knobs" by which control can be achieved.

References

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